19" RACKMOUNT TELCO DATA / PROTOCOL ANALYZER OC3-12/STM-1/4 Analysis and Emulation (& rec/playback) System and Processing of ATM, PoS, ATM/POS Analysis RAW Traffic <u>OC3-T3</u> Record/Playback Capture to Disk DS3/T3, T1/E1 Connectivity RJ-48c BNC ports Gigabit E ports Optical Fiber, RJ-48c, USB Ruggged 2.0, and 19" rackmount Overview Gigabit Ethernet Connectivity Telcom data d) is capable of OC-3/12 and ch as data recording and wirespeed playback of Artivi, Fos, NAW Traine API Toolkit for Specialized The TDA turnkey system comes with software for overall monitoring, BERT, emulation, and protocol analysis with a price tag that compares very favorably with similar test instruments at **Applications Development** three times the price. TDPA OC3-TC is designed for protocol analysis of ATM, PoS, Raw unchannelized and unframed data, and traffic at IP, UDP, and higher layers. The hardware can be easily configured / programmed for delaying of ATM Cells or PPP packets. SONET/SDH/ATM/PoS Alarms The systems's multiple connectivity using Optical Fiber, RJ-48c, Gigabit Ethernet (GigE), and USB 2.0, makes multi channel monitoring a snap. And with removable SSD and upto 16GB of and Error Logging memory there is no hiccups in testing, monitoring, recording or playback performance **Main Features** Emulation & Analysis of PPP Aultiple ports per system for super high capacity monitoring and test system. Hardware gh performance PCIe bus interface with optimized DMA to perform Rx and Tx Features (IP and Higher Layers) packets to/from PC memory. rdware based precise time-stamping of cells with 10 nsec resolution, 1 ppm accuracy. ATM (AAL0, AAL2, AAL5) and ftware selectable OC-3(STM-1) or OC-12(STM-4) for ATM, PoS or Analyzer Transparent Traffic. UMTS Protocol Analysis Features I Toolkit to develop user specific applications. Virespeed processing of ATM, PoS or RAW data for Tx and Rx for both ports. BERT over ATM, PoS, and Traffic recisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 mSec. **RAW formats** ility to capture/playback to/from disk at full rate in both directions for both ports for detailed offline analysis. **Multiple 128-bits Filters** nultaneous synchronous capture or transmit is possible on both optical ports. mprehensive transmit/receive testing capabilities; transmitting and verifying data with incrementing sequence numbers with each packet/cell. Precise Time-stamping sy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, BERT and RAW Packet Delay Emulation M (AAL2, AAL5) Protocol Analyzer Protocol Testing otocol Analysis P (IP and higher layer protocols) Protocol Analyzer Up to 16 GBytes of memory *Units equipped with PCIe card only Cepoint Networks, LLC E-mail: sales@cepoint.com Phone: (603)883-Cepoint 7979 ext. 103 © 2012 Courtesy Trademarks are properties of their respective owners, GL communications, Microsoft corp, Intel Corp, Cepoint Networks, LLC..

Page 2 PoS Analyzer– Packet Over SONET / SDH

Overview

PoS, or Packet over SONET / SDH—OC-3/STM-1 and OC-12/STM-4 is supported at full rates over dual interfaces. Access, capture, analysis, and emulation of PPP and HDLC, all carrying IP traffic in real-time makes this card useful to many applications including routing, deep packet inspection, and other internet traffic applications.

PoS Protocol Analysis

PPP Analyzer can be used to capture a host of PPP protocols exchanged between the two nodes over SONET/SDH link. User can obtain detailed analysis of higher later protocols (IP, TCP, UDP, HTTP, FTP, POP3 etc) and can perform various statistics measurements. Integrated Packet Data Analysis (PDA) in Realtime PPP Analyzer is an outstanding tool for live monitoring of VoIP traffic. It can segregate IP traffic into SIP / H323 / Megaco / MGCP calls and collects statistics, CDRs, ladder diagrams, and a host of other useful information about VoIP calls.

1	<u> </u>	50	Jan 19 19 19 19 19 19 19 19 19 19 19 19 19	-	and an interest of the local division of the			GoTo		_
Dev	TS	Frame#	TIME (Relative)	Len	PPP Layer3Prot	Source IP Add:	Destination IP Ad	UDP Source	UDP Destination	Ľ
42	0	0	00 00 00 000000000	1030	Internet Protocol	192 168 1.111	192.168.1.222	20001	10001	1
2	0	1	00:00:00.000013770	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	2	00:00:00.000027640	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	3	00:00:00.000041410	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	4	00:00:00.000055270	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	5	00.00.00.000069050	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	6	00:00:00.000082910	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	7	00:00:00.000096770	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
2	0	8	00:00:00.000110550	1030	Internet Protocol	192.168.1.111	192.168.1.222	20001	10001	
Pro Ver In	Fram otoco rsion terne	e Data + PPP 1 IP t Header	Frame=0 at 00:0 FCS Link Layer === Layer ====== Length (In 32			00 00100001	Internet Prot	tocol		-
Ver In Ty D	Fram otoco rsion terne pe of reced elay hroug	e Data + PPP I I I I I I I I I I I I I I I I I	FCS Link Layer Layer		 - 000000 - 0100 01 - 000 0	00 00100001	lay roughput	tocol		
Ver In Ty PD T	Fram otoco rsion terne pe of reced elay hroug eliab	e Data + PPP 1 IP t Header Service ence hput ility	FCS Link Layer === Layer ==== Length (In 32		 - 000000 - 0100 01 - 000 0	000 00100001 (4) .01(5) Routine Normal De Normal Th	lay roughput	tocol		
Ver In Ty PD T	Fram otoco rsion terne pe of reced elay hroug eliab	e Data + PPP 1 IP t Header Service ence hput ility	FCS Link Layer Layer			000 00100001 (4) .01(5) Routine Normal De Normal Th	lay roughput liability	tocol		*

Figure: PPP Protocol Analyzer

PoS Port Configuration

PoS Port Configuration allows users to select FCS type, control FCS stripping on Rx and FCS appending on Tx.

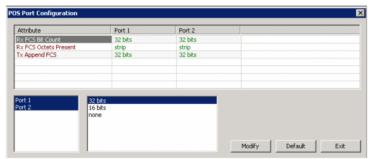


Figure: PoS Port Configuration



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PoS BERT

Support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, status for pattern sync, bit errors counters, and packet rate and packet gap configuration options, configurable header lengths and header information.

Verse Windows Holp	ats: Port 1 +						
Configurations	Tx Config		ŧ×	Rx Config			
Part I Bert - Tx Tx Config Rx Config	a second second second second	P To its counted sett Pastoad Traffic Rate Inp		Port Selection Port 2	Proceediations Percent		
Results Statistics Part 2 V Best I Res Tx Config Results Satistics				BERT Configuration BER Pattern [2014] 31 User Define Al Overs [1 Al Zero	5 _ bits	Sync Declare Settings Sync Achieve Declare Count 56 Sync Loss Declare Count 5 Sync Loss Declare Window 1000 Accesses SetGa/C	
statements	Results		₽×	Statistics			
	Port Selection Port 1	* Reset Clear LED	History Treet Error	Port Selection Port 1	* Reset.Ru		
	Dert Statue			Tx	Values	Rx	Values
	Richo Traffic	Not Active		Frame count	10 10 10 10 10 10 10 10 10 10 10 10 10 1	Total frame count	925622
	Seric Less	Mit Active		Dyte count		This frame count	925022
	BR Drive	Not Active				IP checksum error count	0
	Out of Sequence Packet	 Not Active 				3Pv6 frame count	0
						Non IP test frame count	0
	Bert Satisfica	Values				IF data over IF lever frame count.	0
	BERT STATUS	SINC				UDP data over IP layer frame count	925023
	Test Time	00-00-32				TCP data over IP layer frame count	0
	No Re Data Count	0.00.52				3CHP data over IP layer frame count	0
	No Rx Data Seconds	0				30PP data over IP layer frame count	
	Fills Received	299125200				3GPP data over 3P layer frame count.	0
	BR BYOY COURT	0				Other data over IP layer frame count	0
	DE Error Ratio	D.0000E4000				UDP checksum error frame count	0
	DR Drog Seconds	D				UDP frame count	0
	Out Of Seq. Count	D				Non UDP test frame count	0
Stap Tx	Song Loss Court	6				A 2010 10 10 10 10 10 10 10	
	Sanc Lass Seconds						
Stop Fx	Error Free Seconds	33					

Figure: PoS BERT

PoS Tx / Rx Test

An emulation and test capability that transmits fixed, random, or variable lengths test packets and checks packets on receive at a user specified data transmission rate

Rx Port	Statistics		Rx		
<u>v</u> 2 <u>v</u>	Packets	5 973	Packets		5 841
ngth without FCS Fix/Var Packet Length					
Min: 20 Fixed	Bits/Sec	4 070 880	Bits/Sec		3 980 416
Max: 1000 Var. Random	Pkts/Sec	990	Pkts/Sec		968
Fixed: 203	Percent	2.739	Percent		2.678
c Config (max: 148.608 Mbps) Packets/Sec I000 Bits / Sec Percent	Rx Seq Er		0 R×L	Inderrun Count	0
Packets/Sec 1000 Bits / Sec Percent 4 080 000 2.767		in Count		Inderrun Count —	ō
Packets/Sec 1000 Bits / Sec Percent 4 080 000 2.767	Rx Error Statistic I	in Count	0	Inderrun Count	0 Err %
Packets/Sec 1000 Bits / Sec Percent 4 080 000 2.767	Tx Over	in Count	0		Err %
Packets/Sec 1000 Bits / Sec Percent 4 080 000 2.767	Rx Error Statistic I Packet Length 1-10 11-50	un Count uckets Total Co	0 unt 0 186	Error Count 0 0	Err % 0.000 0.000
Packets/Sec 1000 Bits / Sec Percent 2.767 epend Fixed Length Header Octets (Hex)	Rx Error Statistic I Packat Length 1-10 11-50 S1-200	uckets	0 unt 0 186 500	Error Count 0 0 0	Err % 0.000 0.000 0.000
Packets/Sec 1000 Bits / Sec Percent A 080 000 Percent Sec 1000 Percent	Rx Error Statistic 1 Packet Length 1-10 11-50 51-200 201-500	uckets Total Co	0 unt 0 186 500 500	Error Count 0 0 0 0	Err % 0.000 0.000 0.000 0.000
Packets/Sec 1000 Bits / Sec Percent A 080 000 Percent Percent C.767 epend Fixed Length Header Octets (Hex) CError Statistic Length Buckets (space separated) 10 50 200 500 2000 None	Rx Error Statistic I Packat Length 1-10 11-50 S1-200	uckets Total Co	0 unt 0 186 500	Error Count 0 0 0	Err % 0.000 0.000 0.000 0.000 0.000
Packets/Sec 1000 Bits / Sec 1000 Bits / Sec 1000 Percent 2.767 epend Fixed Length Header Octets (Hex) c Error Statistic Length Buckets (space separated) 10 59 200 500 2000 Nove 100	Tx Overn Rx Error Statistic I Packet Length 1-10 11-50 51-200 501-2000	uckets Total Co	0 unt 0 186 200 200 255	Error Count 0 0 0 0 0	

Figure: PoS Tx/Rx Test

ATM Analyzer- Asynchronous Transfer Mode Over SONET / SDH

Overview

ATM over SONT/SDH— OC-3/STM-1 and OC-12/STM-4 is supported at full rates over dual interfaces. Access, capture, analysis, and emulation of ATM cells at wirespeed make this interface capability applicable for wide ranging next generation networks.

ATM Protocol Analyzer

ATM Analyzer is used to analyze and view ATM protocols across the U-plane for both NNI and UNI interface carrying AALO, AAL2 and AAL5 traffic.

UMTS Protocol Analyzer

UMTS analyzer is capable of capturing, decoding and performing various test measurements across various interfaces i.e. lub, lur, luCs and luPs interfaces of the UMTS network. In addition, it supports ATM as the transport layer. It helps in fault diagnosis and troubleshooting UMTS network.

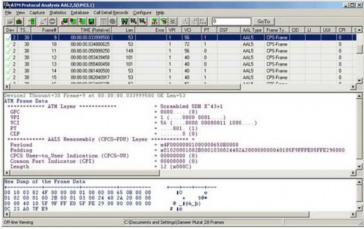


Figure: ATM Protocol Analyzer

ATM Configuration

ATM Configuration allows user to either pass or drop the Idle cells at the receiving stream.

× Pass / Drop Idle Cells —	OK
Use Ctrl key for selection	Cancel
Port1: DROP Port2: DROP	

ATM BERT

Support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, All one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, HEC error insertion, on receive filtering is provided for idle cells, GFC, VPI, VCI, CL, and PT cells, statistical details for total cells, valid cells, idle cells, filtered cells, and filtered out cells.

- File New Windows	THE						- 0 >
088 * ×	Porte: Port 1 +	1					
Configurations	Tx Config			Re Cordig			# 3
B Port 1 B # Bert - Tx Tx Config #x Config		Fasted State Rate Sector		Port Selection	Port 2 💌 🗗 To 5. Ref Parload		
Pot 2 Pot 2 Pot 2 Reads Pot 2 Reads Reads Statistics	EERT Configuration BER Pattern [2013- 31 User Def [2010ers] 20120 [2010ers] 20120	tergith	Her Configuration Her Configuration				
	Reads		¢×	Ratistics			
	Part Selection Part	Reset GearLED History Street Error		Port Selection	Port 1 Passat R	×	
	Dert Status			Ts	Values	Its Values	
Stort R. Stop Re	Ric No Traffic Sync Lass Bt Ever	Not Active Not Active Not Active		Prane count Dyte count	-	Total cell count 2912921 3de cell count 0 BDR set cell count 2912922 Filtered cut cell count 0	
	Pert Statutes DERT Statue Test Time Ho Ro Data Goant Ho Ro Data Secundo Bit Fine Court Bit Fine Court Bit Fine Rate Bit Fine Rate Bit Fine Secundo Stricture Court	Volume 57%C 00.014.21 1105694982 0 0 0				HDC error count 0	
1	Sync Less Seconds Envir Pree Seconds	1					

Figure: ATM BERT

ATM Tx / Rx Test

An emulation and test capability that transmits ATM test cells and / or analyzes the received cells at a user specified data transmission rate

Bits / Sec Percent Insert En	Tx Port	Rx Port User/Network Interface	Tx Config (Cells/Sec	max 148 Mbps, 353 Ko 30000	ps)	Pause Tx	Stop
ATM Header Fields III 2 200 000 8.494 Reset En GPC 5 Cenest: Flow Control (0:10) 5 Ext VPI 30 Vrtuil Parth Isteritier (0:255) Fax Ext VEI 555 Vrtuil Clerryler (0:055557) Fax Cells 12 250 308 Ext PT 0 Payload Typel (0:7) Extension Ext Parcent 8.459 Percent 0 CIP 0 Cell Loss Priority (0:1) Fax Seq Envire Count P Percent 0 Percent P Percent P Percent P Percent P	1	none 💌 🤄 UVII. C MIII		1	Percent		Insert Erro
Statistics Pax Text Cells 0 VCI 555 Vrtuil Channel Dem/Her (0-55557) Text Cells PT 0 Psychold Typel (0-7) Deschold Typel (0-7) Parcent 8-429 Percent 0 Results Results Rx Seq Resync Count 0 Rx Underum Count Rx Underum Count	ATM Header Fields				8.494		Reset Error
VPI 20 VFLuid Purkt Serrifer (0, 055) VCI 055 VFLuid Clerryet Identifer (0, 055307) PT 0 Parksot Typel (0-77) CLP 0 Cell Loss Priority (0-57) PT 0 Cell Loss Priority (0-57) Results 12.629 0 Results Results 0 Percent 8.429 Percent Results Fox Seq Resync Count 0 RX Seq Resync Count 0 0	GPC 5	Generic Flow Control (0-15)	Timer 33 r				Exit
VPI 0 VP1ull Outrie Parth Identifier (0:0555) VCI VP1ull Outrie Outrie (0:05555) Test Cells 0 PF 0 Paylood Typel (0:7) EtailSec 122760 Test Cells 0 CLP 0 Cell Loss Priority (0:1) Results RX Seq Resync Count P Results RX Seq Resync Count P Rx Underrun Count Rx Underrun Count					- Pv		
VCI S55 Vrtual Cherniel Identifier (0-55555) PT 2 Psychod typel (0-7) CLP Cell Loss Priority (0-1) Results Rs see Resync Count Rx See Resync Count P	VPI 20	Vetual Path Identifier (0.255)		122 760		0	
PT D Psyload type!r (0-7) Bits/Sec D Cell/Sec D CLP Cell/Loss Privrty (0-5) Percent 8-429 Percent D Results Rs Seg Resync Count P Rs Seg Resync Count P Rs Underrun Count					Total Cells	0	
PT 0 Psyload Typel (0-7) CLP 0 Cellulose Priority (0-3) Results Results Percent Percent Results Percent Percent<	VCI 655	Virtual Channel Identifier (0-65535)	Bits/Sec	12 623 328	Bits/Sec	0	
CLP 0 Criticos Prorty (0-1) Results R	er 0	Tendend Turnel (T. 7)	Cells/Sec	29 772	Cells/Sec		
Results Rx Seq Resync Count P Rx Seq Error Count P Rx Seq Error Count Rx Underrun Count	r. 1-		Percent	8.429	Percent	0	
Rx Seq Resync Court P Rx Seq Error Court P Tx Overan Court Rx Underrun Court	CLP 0	Cell Loss Priority (0-1)					
Rx Seg Error Count P Tx Overnun Count Rx Undernun Count				Sea Resvoc Count	b		
Tx Overrun Count Rx Underrun Count							-8
p p					Rx Und	errun Count	
			jo		0		
R× DTE Error Count			RU				



Figure: ATM Port Configuration



Other Applications of OC3-T3 Analyzer

Page 4

Record, Playback Packets and Cells

These modules allow users to transmit and capture packets from file or to a file over OC-3/STM-1 and OC-12/STM-4 interfaces. Offline utility can convert it into GL's HDL file format or PCAP format.

Transmit Packets from File

- ansmits packets / cells from the file.
- ckets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF).
 - ansmit packets/cells at a user configurable rate.
- ansmits on the same port as captured, swaps ports or uses a specified port.
- ovides the statistics of the transmitted cells at both line level and payload level.
- ansmit packets synchronously on multiple boards

Receive Packets to File

ardware provided **versatile multiple filters** can be applied to incoming data on each individual port to allow traffic of interest only. ATM and PoS traffic can be filtered at hardware level to target traffic of interest only.

lows Wirespeed capture of all payload from SONET/SDH envelop transparent of transport level.

ptures the received packets synchronously on multiple boards into a file up to hard drive capacity.

ckets can be captured continuously (till user manually stops the capture or up to hard drive capacity) or limited by a specified size in MB, a packet count, or a specified time limit.

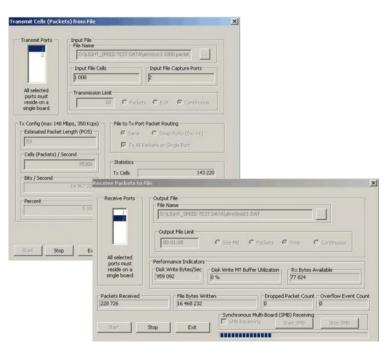


Figure: Receive Packets to File, Transmit Packets from File



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Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

x Under	rRuns (Source (Rx)	Destinat		
		1,2	1,2	-	Start
x OverF	Runs				Stop
Packe	t Mode	Skip Rx and Tx On1	imer (pause)	(mit)	
Page	Mode	Flush Tx After Each	Packet Tx (p	acket mode)	
x inform	nation		Tx inform	nation	
Port	Packets	Bytes	Port	Packets	Bytes
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
1,2	1 836 430	102 840 080	1,2	1 836 430	102 840 080
		102 840 080	1,2	1 836 430	102 840 080
	Avail LB:		1,2	1 836 430	102 840 080
x Bytes x Free S		16	1,2	1 836 430	102 840 080
x Bytes x Free S	Avail LB: ipace LB:	16 52 260 879	1,2	1 836 430	102 840 080
× Bytes × Free S × Free -	Avail LB: ipace LB:	16 52 260 879	1,2	1 836 430	102 840 080

Figure: Memory Loopback

Alarms and Errors Counters Monitoring

The alarms and error monitoring window provided for each of the OC-3/OC-12 port displays detailed status of the communication with the other end.

Hardware LEDs are provided on the card to read line alarms.

Monitored Alarms and error counts include –

- he errors such as OOF, LOS, LOF, AIS, RDI, and APSBF
- S, Rx / Tx Abort, and MIN / MAX Length he, Path, and Section
- error counts

Alarms	👪 Monitor #1 📰 🖬
OOF LOF LOS AIS RDI APSBF	Alarms ODF LOF LOS Als
Eirors Section BIP O Line BIP O Line REI O Path BIP O Path REI O FCS O MIN Length O MAX Length O Tx Abort O	Enors Section BIP 0 Line BIP 0 Line REI 0 Path BIP 30 Path REI 0 HEC 0
Reset All Hide Panel	Reset All Hide Panel

Page 5 Other Applications of OC3-T3 Analyzer

SONET/SDH RAW (or Transparent) Payload

Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications. Current applications include:

W BERT – support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^{-1} to 10^{-9} , status for pattern sync, and bit errors counters.

irespeed capture of raw data to hard disk on one or both ports simultaneously. The data is recorded in 64 bytes block with appropriate header.

ayback of recorded data from file at wirespeed on one or more ports.

arms and Error monitoring and logging at SONET/SDH level.

Performance Counters

Following performance counters are available in the analyzer: Tx Statistics, Rx Statistics, PMC TxRx Statistics, Interrupt Statistics, and DMA Engine

The statistics display two types of counters: board counters and port counters. The board counters display cumulative counts for all ports on the same board, while port counters display information for each port separately.

Tx Descripl Rx Descrip Application Tx Laps Rx Laps	Board Cour DMA TX Inte DMA RX Inte DMA Terrer 1	-	tics Restatistics				X
A Duffer L Tx Buffer L Tx Buffer 1 Tx Buffer 1 Tx Buffer 1 Tx Buffer 1 Tx Buffer 1 Tx Buffer 1 Tx Buffer 1	DMA Trave 1 OMA 72 Into OMA 72 Into OMA There 1 Force Statis	DMA Eng DMA Eng PC Memic DTE Pack DTE Gig INTF Gig INTF Gig INTF Gig INTF Gig INTF Gig INTF Gig DTE Pack	Board Countery DMA Engine PC DMA Engine PC DTE Packets DTE Gagt PKTs INITF Gagt PKTs INITF Gagt PKTs INITF Gagt Max I INITF Gagt Max I	e Packets e Pgs ed PKTs per Sec en PKTs	Board 1 192 668 918 3 391 681 192 195 103 0 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605 3 735 936 605		
Refrest		INTE Pac INTE Errc INTE Pac	Port Counters DTE OC-3/12 I 3VTF OC-3/12 3VTF OC-3/12 3VTF OC-3/12 3VTF OC-3/12 3VTF OC-3/12 Filtered OC-3/1 Filtered OC-3/1 Filtered OC-3/12 Filtered OC-3/12 Elibert OC-3/12 Elibert OC-3/12	Port Counters TX cells RX idle cells RX cells RX HCS errors		Port 1 4 996 949 960 059 015 187 240 772 0	Port 2 187 203 069 1 138 319 674 5 427 366 4

Figure: Packet Delay Emulation

Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

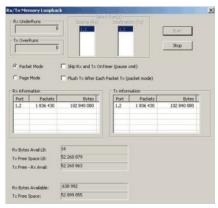


Figure: Memory Loopback

Packet Delay Emulation for PoS and ATM based traffic The Network Delay Emulator is an optional application (requires license) provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms. The application combines hardware and software based functions to achieve precision and flexibility. It can emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic.

With this application, the user can:

- st the impact of delay and congestion under various real world conditions,
 - sess impact of delay on SLA (Service Level Agreements),
 - nulate satellite delay and long Fiber Loops

st WAN application performance under deteriorated but repeatable conditions

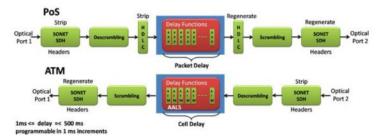


Figure: Packet Delay Emulation



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SPECIFICATIONS^{*}

OC3, T3, T1/E1 Physical Connectivity Interfaces

OC-3/STM-1: SC Connector STS-1/STM-0/T3: Male BNC Connector T1/E1: RJ48c Connector External Clock: MCX Connector PC Interface: PCI 2.1 Compliant OC-3/STM-1 Line Interface Physical Interface: SC Connector Fiber Pigtail: Single mode, 1310 nm Pulse Mask: Meets ITU-T G.957 and Bellcore DR-253-CORE Line Code: NRZ Output Clock Reference: Recovered OC-3 Clock, External 19.44 MHz, or Internally Generated 155.52MHz ± 4.6 ppm Rx Sensitivity: -31 dBm STS-1/STM-0 Line Interface Physical Interface: BNC Male Connectors Output Clock Reference: Recovered STS-1/STM-0 Clock, External 19.44 MHz, or Internally Generated 51.84MHz ± 4.6 ppm T3 Line Interface Physical Interface: BNC Male Connectors Line Code Format: B3ZS Framing Format: M23, C-bit Input Frequency: 44.736 Mbps Receiver Interface: DSX-3 (Terminate or Monitor) Input Impedance: 75 Ohms Input Level: Terminate- 0.09 Vp – 0.85 Vp Monitor 0.025-0.08 Vp (Up to 26 dB flat loss relative to nominal DSX) Output Level: DSX- Per TR-TSY-0004999, 0.75 to 0.85 Vp Output Clock Source: Recovered or Internal T1/E1 Line Interface Physical Interface: RJ48c Connector Line Code Format: AMI or B8ZS (T1), HDB3 (E1) Input Frequency: 1.544 Mbps (T1) or 2.048 Mbps (E1) Receiver Interface: Terminate Input Impedance: 100 Ohms (T1), 120 Ohms (E1) Input Level: +75 mV to 6.0V base to peak or -30 dBsX to +6 dBsX Output Level: +3.0 +/-0.2 Base to Peak Selectable 0 to 655 ft. Pulse Equalization Setting for T1 Short Haul, or line build outs for 0 dB to -22.5 dB (T1 Long Haul) External Clock Interface Physical Interface: MCX Connector Electrical Standard: RS485/RS422 SONET/SDH Framing Formats SONET: STS-3, STS-3c, STS-1 SDH: STM-1 (AU-3, AU-4) Payload Mappings SONET • STS-3c (Bulk Filled) OC-3 • STS-1 OC-3 (Add/Drop) STS-1 (Bulk Filled) STS-1 • T3 OC-3 (Internal and Add/Drop) • T3 STS-1 (Internal only) • E1 VT-2 STS-1 (Internal and Add/Drop) • E1 VT-2 OC-3 (Internal and Add/Drop) • T1 VT-1.5 STS-1 (Internal and Add/Drop)

SDH

- VC-4 (Bulk filled) AU-4 STM-1
- STM-0 AU-3 STM-1 (Add/Drop)
- VC-3 (Bulk Filled) AU-3 STM-1
- T3 AU-3 STM-1 (Internal and Add/Drop)
- T3 AU-3 STM-0 (Internal only)
- E1 TU-12 TUG-2 AU-3 STM-0
- E1 TU-12 TUG-2 AU-3 STM-1
- E1 TU-12 TUG-2 TUG-3 AU-4 STM-1
- T1 TU-11 TUG-2 AU-3 STM-0
- T1 TU-11 TUG-2 AU-3 STM-1

Other capabilities:

Monitor incoming TOH, POH. Monitor incoming APS messages (K1 and K2), Monitor incoming SPE pointers, Count Pointer Justifications, Detect NDF (New Data Flag) etc.

SDH

Alarm Detection: LOS, LOF, MS-AIS, MS-RDI, AU-LOP, AU-AIS, HP-RDI, HP-UNEQ, H4-LOM, TU-LOP, TU-AIS, LP-RDI, LP-UN-EQ

Error Counting: Framing error, B1 BIP, B2 BIP, MS-REI, B3 BIP, HP-REI, BERT errors

Signal Traces and Labels: Regenerator Section trace (J0), Higher Order trail trace (J1), Section sync status (S1), Path signal label (C2), LP Path label (V5)

Other capabilities: Monitor incoming RS-OH, MS-OH and HO-POH, Monitor incoming APS messages (K1 and K2), Monitor incoming AU pointers. Count Pointer Justifications, Detect NDF (New Data Flag) etc.

PDH

Alarm Detection: **T1:** AIS, OOF, RAI **E1:** AIS, OOF, RAI, CAS-MFL, RMFAI **T3:** LOS, FERF, OOF, AIS, IDLE, RED **Add/Drop Capabilities SONET** Add/Drop to/from OC-3: STS-1, T3, E1 or T1

Add/Drop to/from STS-1: T1 or E1

SDH

Add/Drop to/from STM-1: STM-0, T3, E1 or T1 Add/Drop to/from STM-0: T1 or E1

Frequency Measurements

SONET: OC-3 or STS-1 with 1Hz discrimination, 4.6ppm accuracy **SDH:** STM-1 or STM-0 with 1Hz discrimination, 4.6ppm accuracy

PDH Framing Formats

DS3/T3: C-bit Parity, M23 DS1/T1: Unframed, D4, ESF E1: Unframed PCM30 PCM30CRC PCN

E1: Unframed, PCM30, PCM30CRC, PCM31, PCM31CRC

Alarm and Error Logging

Alarms and Errors can be logged continuously to a file.

Coupled or Independent Settings

Transmit and Receive settings can be set as coupled to change them simultaneously or they can be set as independent.



Cepoint Networks, LLC E-mail: sales@cepoint.com Phone: (603)883-7979 ext. 103 © 2012 Courtesy Trademarks are properties of their respective owners, GL communications, Microsoft corp, Intel Corp, Cepoint Networks, LLC.

Supported Protocols	Available Softwares
M – Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.	OC-3 / STM-1 Related Software
P over SONET (PoS) – Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).	LTS200 – OC-3 / STM-1 ATM Monitor, BERT, Tx/Rx Test, RAW LTS201 – OC-3 / STM-1 PoS Monitor, BERT, Tx/Rx Test, RAW
C-3/OC-12/STM-1/STM-4 Transparent Payload – Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols.	LTS202 – OC-3 / STM-1 ATM and RAW Record / Playback
System config example Interfaces:	LTS204 – OC-3 / STM-1 ATM Protocol Analysis
ual /Quad Ports	LTS205 – OC-3 / STM-1 PoS Protocol Analysis
OC-3 / STM-1 / OC-12 / STM-4 Gigabit Ethernet	LTS206 – OC-3 / STM-1 UMTS Protocol Analysis
ngle Mode or Multi Mode SFP support with LC connector USB 2.0	LTS207 – Delay Emulation for OC3 / STM1 PoS payloads
cols:	LTS208 – Delay Emulation for OC3 / STM1 ATM payloads
C 2615 compliance PoS compliance specs needed	OC-12 / STM-4 Related Software
Tx Clock	LTS300 – OC-12 / STM-4 ATM Monitor, BERT, Tx/Rx Test, RAW
Internal or Recovered	LTS301 – OC-12 / STM-4 PoS Monitor, BERT, Tx/Rx Test, RAW
LOS, LOF, User	LTS302 – OC-12 / STM-4 ATM and RAW Record / Playback
Display Interface:	LTS303 – OC-12 / STM-4 PoS and RAW Record / Playback
VGA/DVI hbedded 8.4" LCD TFT Display	LTS304 – OC-12 / STM-4 ATM Protocol Analysis
Power and Dimensions: Factor: 19" Rackmount	LTS305 – OC-12 / STM-4 PoS Protocol Analysis
0V/230V AC	LTS306 – OC-12 / STM-4 UMTS Protocol Analysis
19" (W) x 22"D x 7" H (4U)	LTS307 – Delay Emulation for OC12 / STM4 PoS payloads
	LTS308 – Delay Emulation for OC12 / STM4 ATM payloads

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