Monitor, Record, Playback, and Processing of ATM, PoS, RAW Traffic

Add and drop T1, E1, T3, STS-1/STM-0 signals to and from an OC-3/STM-1 signal or T1 and E1 signals to and from an STS-1/STM-0 signal

Optical Fiber, RJ-48c, USB 2.0, and Gigabit Ethernet Connectivity

API Toolkit for Specialized Applications Development

SONET/SDH/ATM/PoS Alarms and Error Logging

Emulation & Analysis of PPP (IP and Higher Layers)

ATM (AAL0, AAL2, AAL5) and UMTS Protocol Analysis

BERT over ATM, PoS, and RAW formats

Multiple 128-bits Filters

Precise Time-stamping

Packet Delay Emulation

Up to 16 GBytes of memory

19" RACKMOUNT TELCO DATA / PROTOCOL ANALYZER

OC3-12/STM-1/4 Analysis and Emulation (& rec/playback) System

ATM/POS Analysis

OC3-T3

Record/Playback

Capture to Disk

DS3/T3, T1/E1 Connectivity

RJ-48c

BNC ports

Gigabit E ports

Ruggged 19" rackmount

Overview

Telcom data [redacted]d) is capable of OC-3/12 and S[redacted]ch as data recording and wirespeed playback of ATM, PoS, RAW Traffic.

The TDA turnkey system comes with software for overall monitoring, BERT, emulation, and protocol analysis with a price tag that compares very favorably with similar test instruments at three times the price. TDPA OC3-TC is designed for protocol analysis of ATM, PoS, Raw unchannelized and unframed data, and traffic at IP, UDP, and higher layers. The hardware can be easily configured / programmed for delaying of ATM Cells or PPP packets.

The systems's multiple connectivity using Optical Fiber, RJ-48c, Gigabit Ethernet (GigE), and USB 2.0, makes multi channel monitoring a snap. And with removable SSD and upto 16GB of memory there is no hiccups in testing, monitoring , recording or playback performance

Main Features

Hardware Features

- [redacted]ultiple ports per system for super high capacity monitoring and test system.
- [redacted]gh performance PCIe bus interface with optimized DMA to perform Rx and Tx packets to/from PC memory.
- [redacted]rdware based precise time-stamping of cells with 10 nsec resolution, 1 ppm accuracy.

Analyzer Features

- [redacted]ftware selectable OC-3(STM-1) or OC-12(STM-4) for ATM, PoS or Transparent Traffic.
- [redacted]I Toolkit to develop user specific applications.

Traffic

- [redacted]Wirespeed processing of ATM, PoS or RAW data for Tx and Rx for both ports.
- [redacted]recisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 mSec.
- [redacted]ility to capture/playback to/from disk at full rate in both directions for both ports for detailed offline analysis.
- [redacted]multaneous synchronous capture or transmit is possible on both optical ports.
- [redacted]mprehensive transmit/receive testing capabilities; transmitting and verifying data with incrementing sequence numbers with each packet/cell.

BERT

- [redacted]sy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, and RAW

Protocol Testing

- [redacted]M (AAL2, AAL5) Protocol Analyzer
- [redacted]otocol Analysis
- [redacted]P (IP and higher layer protocols) Protocol Analyzer

*Units equipped with PCIe card only

Cepoint Networks, LLC E-mail: sales@cepoint.com Phone: (603)883-7979 ext. 103

PoS Analyzer– Packet Over SONET / SDH

Overview

PoS, or Packet over SONET / SDH—OC-3/STM-1 and OC-12/STM-4 is supported at full rates over dual interfaces. Access, capture, analysis, and emulation of PPP and HDLC, all carrying IP traffic in real-time makes this card useful to many applications including routing, deep packet inspection, and other internet traffic applications.

PoS Protocol Analysis

PPP Analyzer can be used to capture a host of PPP protocols exchanged between the two nodes over SONET/SDH link. User can obtain detailed analysis of higher later protocols (IP, TCP, UDP, HTTP, FTP, POP3 etc) and can perform various statistics measurements. Integrated Packet Data Analysis (PDA) in Real-time PPP Analyzer is an outstanding tool for live monitoring of VoIP traffic. It can segregate IP traffic into SIP / H323 / Megaco / MGCP calls and collects statistics, CDRs, ladder diagrams, and a host of other useful information about VoIP calls.

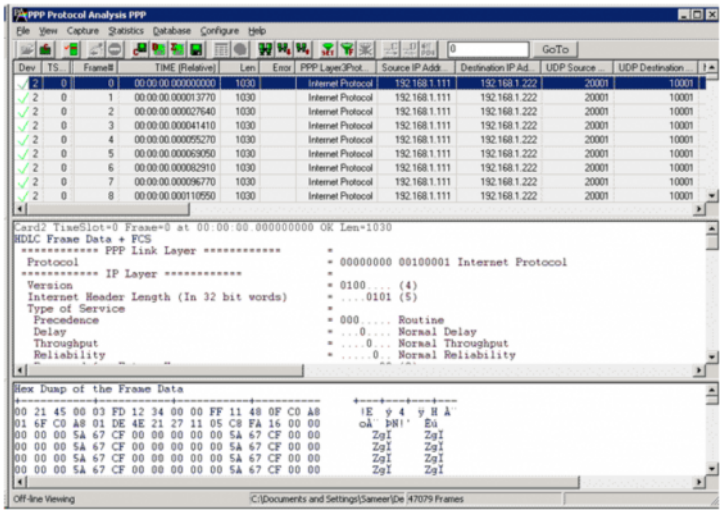

Figure: PPP Protocol Analyzer

PoS Port Configuration

PoS Port Configuration allows users to select FCS type, control FCS stripping on Rx and FCS appending on Tx.

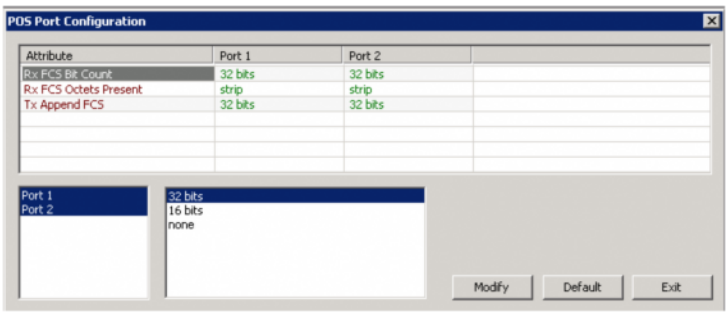

Figure: PoS Port Configuration

PoS BERT

Support for the following PRBS Patterns: 2^9 – 1, 2^11 – 1, 2^15 – 1, 2^20 – 1, 2^23 – 1, 2^29 – 1, 2^31 – 1, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, status for pattern sync, bit errors counters, and packet rate and packet gap configuration options, configurable header lengths and header information.

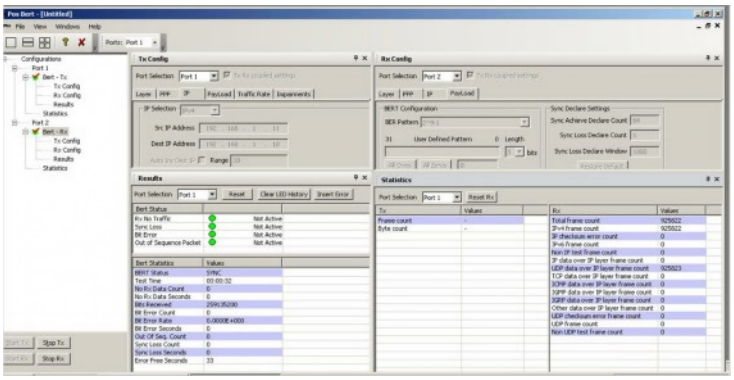

Figure: PoS BERT

PoS Tx / Rx Test

An emulation and test capability that transmits fixed, random, or variable lengths test packets and checks packets on receive at a user specified data transmission rate

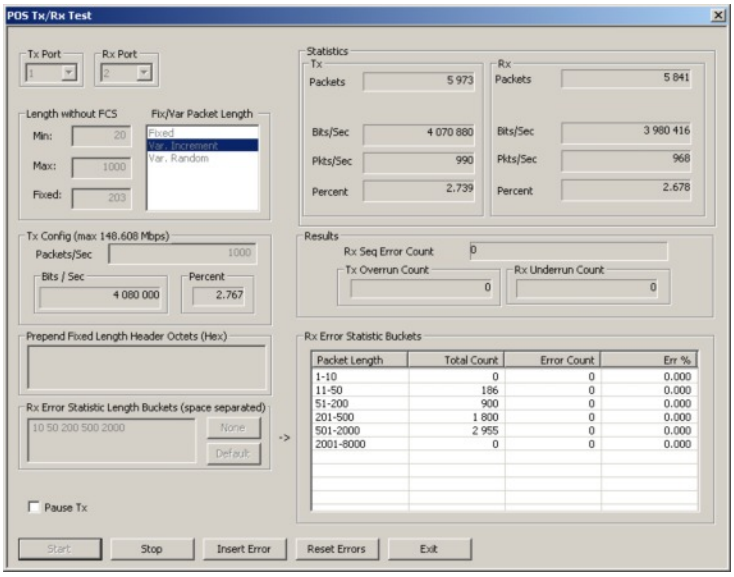

Figure: PoS Tx/Rx Test

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ATM Analyzer– Asynchronous Transfer Mode Over SONET / SDH

Overview

ATM over SONT/SDH— OC-3/STM-1 and OC-12/STM-4 is supported at full rates over dual interfaces. Access, capture, analysis, and emulation of ATM cells at wirespeed make this interface capability applicable for wide ranging next generation networks.

ATM Protocol Analyzer

ATM Analyzer is used to analyze and view ATM protocols across the U-plane for both NNI and UNI interface carrying AAL0, AAL2 and AAL5 traffic.

UMTS Protocol Analyzer

UMTS analyzer is capable of capturing, decoding and performing various test measurements across various interfaces i.e. Iub, Iur, IuCs and IuPs interfaces of the UMTS network. In addition, it supports ATM as the transport layer. It helps in fault diagnosis and troubleshooting UMTS network.

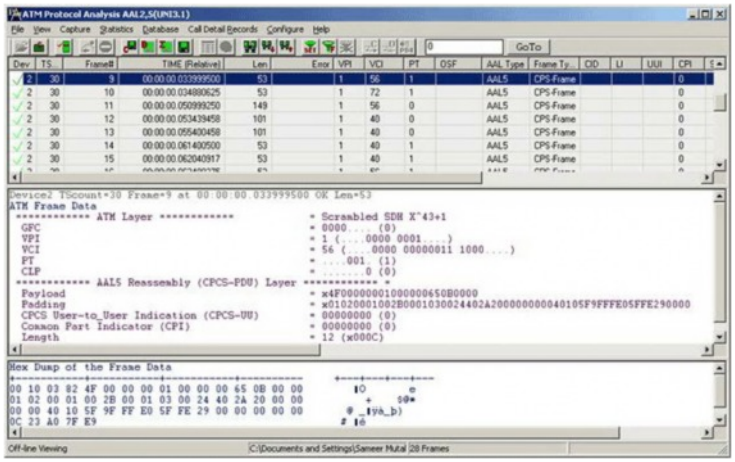


Figure: ATM Protocol Analyzer

ATM Configuration

ATM Configuration allows user to either pass or drop the Idle cells at the receiving stream.

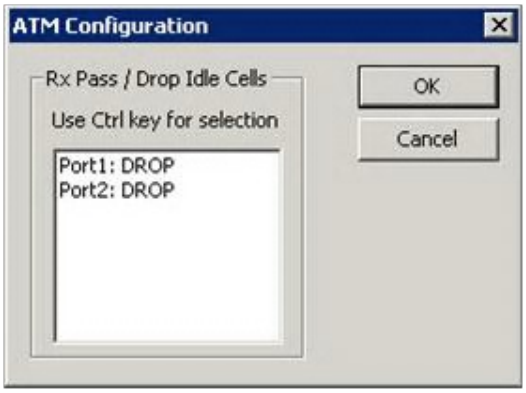


Figure: ATM Port Configuration

ATM BERT

Support for the following PRBS Patterns: 2^9 – 1, 2^11 – 1, 2^15 – 1, 2^20 – 1, 2^23 – 1, 2^29 – 1, 2^31 – 1, All one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, HEC error insertion, on receive filtering is provided for idle cells, GFC, VPI, VCI, CL, and PT cells, statistical details for total cells, valid cells, idle cells, filtered cells, and filtered out cells.

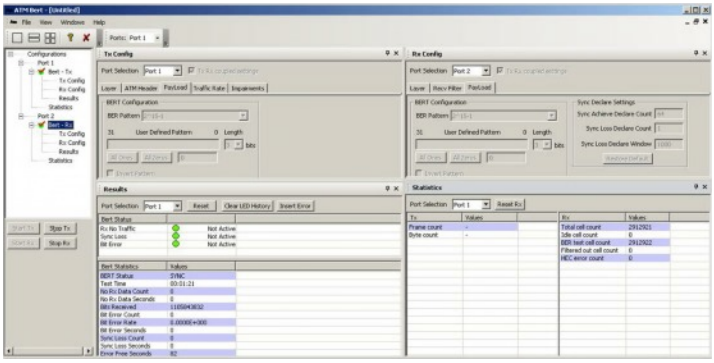


Figure: ATM BERT

ATM Tx / Rx Test

An emulation and test capability that transmits ATM test cells and / or analyzes the received cells at a user specified data transmission rate

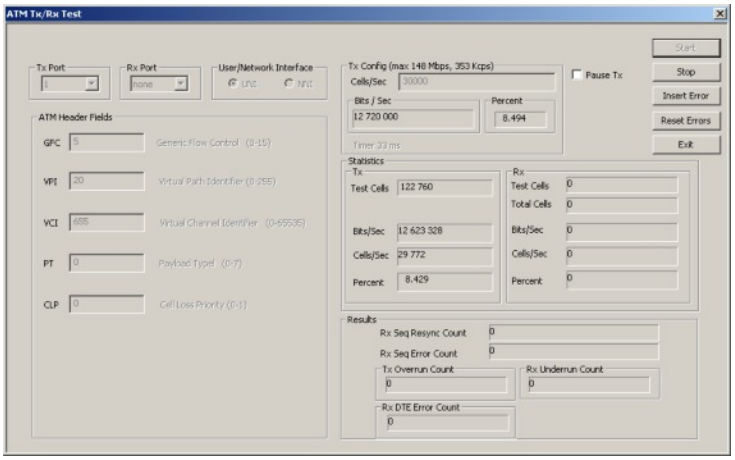


Figure: ATM Tx/Rx Test

Other Applications of OC3-T3 Analyzer

Record, Playback Packets and Cells

These modules allow users to transmit and capture packets from file or to a file over OC-3/STM-1 and OC-12/STM-4 interfaces. Offline utility can convert it into GL's HDL file format or PCAP format.

Transmit Packets from File

- [redacted]ansmits packets / cells from the file.
- [redacted]ckets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF).
- [redacted]ansmit packets/cells at a user configurable rate.
- [redacted]ansmits on the same port as captured, swaps ports or uses a specified port.
- [redacted]ovides the statistics of the transmitted cells at both line level and payload level.
- [redacted]ansmit packets synchronously on multiple boards

Receive Packets to File

- [redacted]ardware provided **versatile multiple filters** can be applied to incoming data on each individual port to allow traffic of interest only. ATM and PoS traffic can be filtered at hardware level to target traffic of interest only.
- [redacted]ows Wirespeed capture of all payload from SONET/SDH envelop transparent of transport level.
- [redacted]ptures the received packets synchronously on multiple boards into a file up to hard drive capacity.
- [redacted]ckets can be captured continuously (till user manually stops the capture or up to hard drive capacity) or limited by a specified size in MB, a packet count, or a specified time limit.

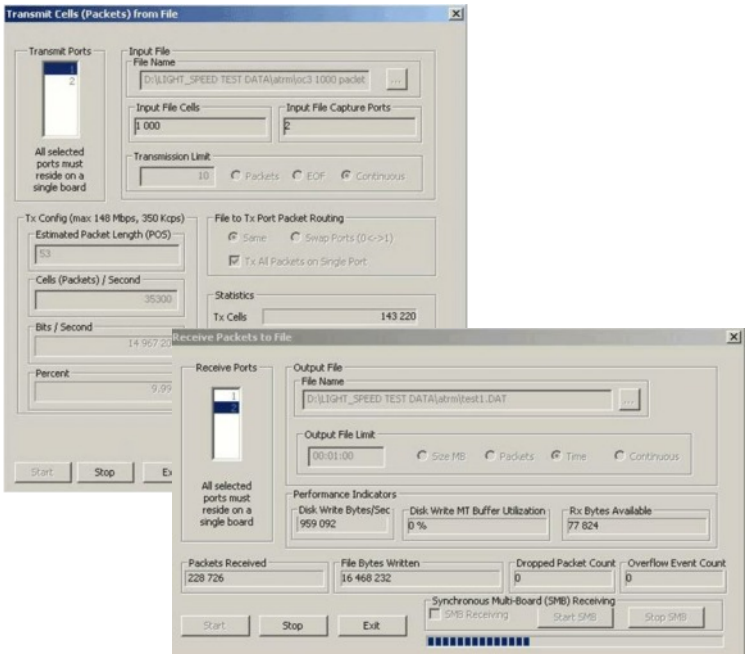


Figure: Receive Packets to File, Transmit Packets from File

Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

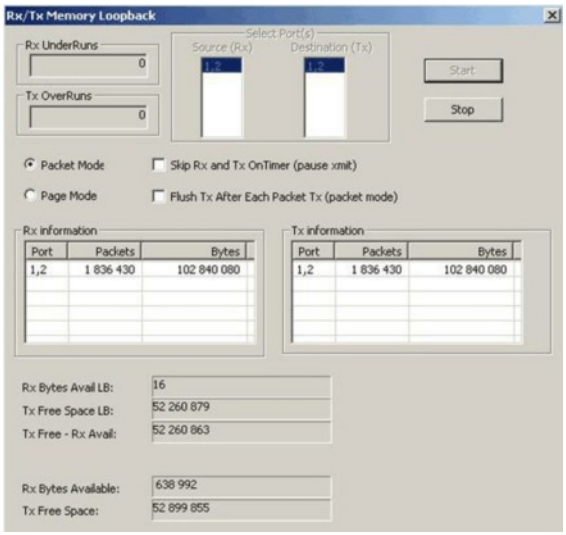


Figure: Memory Loopback

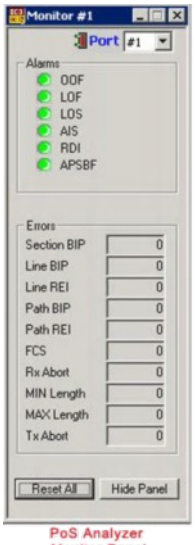
Alarms and Errors Counters Monitoring

The alarms and error monitoring window provided for each of the OC-3/OC-12 port displays detailed status of the communication with the other end.

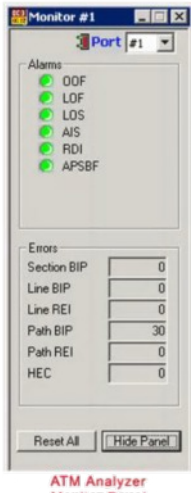
Hardware LEDs are provided on the card to read line alarms.

Monitored Alarms and error counts include –

- [redacted]e errors such as OOF, LOS, LOF, AIS, RDI, and APSBF
- [redacted]S, Rx / Tx Abort, and MIN / MAX Length
- [redacted]e, Path, and Section error counts



PoS Analyzer Monitor Panel



ATM Analyzer Monitor Panel

Other Applications of OC3-T3 Analyzer

SONET/SDH RAW (or Transparent) Payload

Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications. Current applications include:

RAW BERT – support for the following PRBS Patterns: 2^9 – 1, 2^11 – 1, 2^15 – 1, 2^20 – 1, 2^23 – 1, 2^29 – 1, 2^31 – 1, all one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^–1 to 10^–9, status for pattern sync, and bit errors counters.

Wirespeed capture of raw data to hard disk on one or both ports simultaneously. The data is recorded in 64 bytes block with appropriate header.

Playback of recorded data from file at wirespeed on one or more ports.

Alarms and Error monitoring and logging at SONET/SDH level.

Performance Counters

Following performance counters are available in the analyzer: Tx Statistics, Rx Statistics, PMC TxRx Statistics, Interrupt Statistics, and DMA Engine

The statistics display two types of counters: board counters and port counters. The board counters display cumulative counts for all ports on the same board, while port counters display information for each port separately.

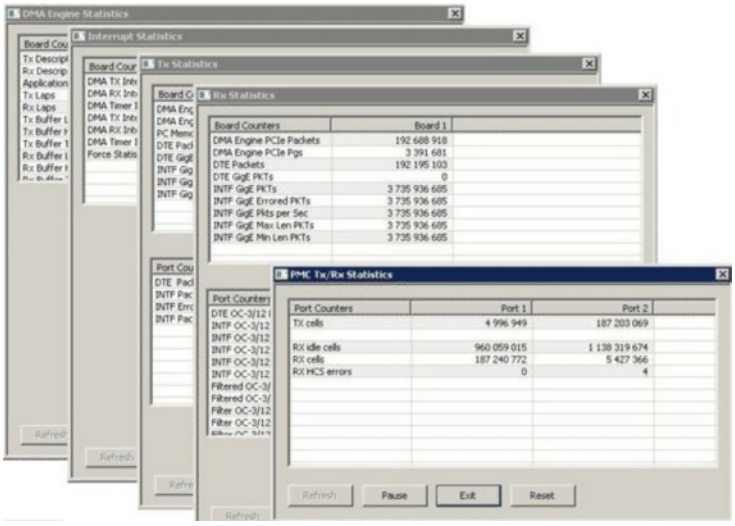


Figure: Packet Delay Emulation

Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

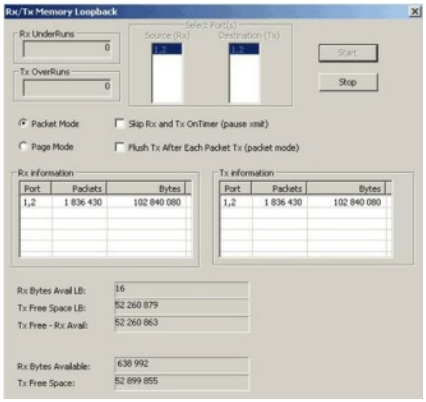


Figure: Memory Loopback

Packet Delay Emulation for PoS and ATM based traffic

The Network Delay Emulator is an optional application (requires license) provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms. The application combines hardware and software based functions to achieve precision and flexibility. It can emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic.

With this application, the user can:

- Test the impact of delay and congestion under various real world conditions,
- Assess impact of delay on SLA (Service Level Agreements),
- Emulate satellite delay and long Fiber Loops
- Test WAN application performance under deteriorated but repeatable conditions

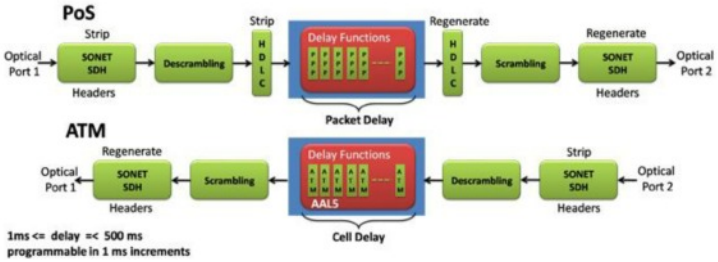


Figure: Packet Delay Emulation

SPECIFICATIONS*

OC3, T3, T1/E1 Physical Connectivity Interfaces

OC-3/STM-1: SC Connector
STS-1/STM-0/T3: Male BNC Connector
T1/E1: RJ48c Connector
External Clock: MCX Connector
PC Interface: PCI 2.1 Compliant

OC-3/STM-1 Line Interface

Physical Interface: SC Connector
Fiber Pigtail: Single mode, 1310 nm
Pulse Mask: Meets ITU-T G.957 and Bellcore DR-253-CORE
Line Code: NRZ
Output Clock Reference: Recovered OC-3 Clock, External 19.44 MHz, or Internally Generated 155.52MHz ± 4.6ppm
Rx Sensitivity: -31 dBm

STS-1/STM-0 Line Interface

Physical Interface: BNC Male Connectors
Output Clock Reference: Recovered STS-1/STM-0 Clock, External 19.44 MHz, or Internally Generated 51.84MHz ± 4.6ppm

T3 Line Interface

Physical Interface: BNC Male Connectors
Line Code Format: B3ZS
Framing Format: M23, C-bit
Input Frequency: 44.736 Mbps
Receiver Interface: DSX-3 (Terminate or Monitor)
Input Impedance: 75 Ohms
Input Level: **Terminate**- 0.09 Vp – 0.85 Vp
Monitor 0.025– 0.08 Vp (Up to 26 dB flat loss relative to nominal DSX)
Output Level: **DSX**- Per TR-TSY-0004999, 0.75 to 0.85 Vp
Output Clock Source: Recovered or Internal

T1/E1 Line Interface

Physical Interface: RJ48c Connector
Line Code Format: AMI or B8ZS (T1), HDB3 (E1)
Input Frequency: 1.544 Mbps (T1) or 2.048 Mbps (E1)
Receiver Interface: Terminate
Input Impedance: 100 Ohms (T1), 120 Ohms (E1)
Input Level: +75 mV to 6.0V base to peak or –30 dBsX to +6 dBsX
Output Level: +3.0 +/-0.2 Base to Peak Selectable 0 to 655 ft. Pulse Equalization Setting for T1 Short Haul, or line build outs for 0 dB to –22.5 dB (T1 Long Haul)

External Clock Interface

Physical Interface: MCX Connector
Electrical Standard: RS485/RS422

SONET/SDH Framing Formats

SONET: STS-3, STS-3c, STS-1
SDH: STM-1 (AU-3, AU-4)

Payload Mappings SONET

- STS-3c (Bulk Filled) □□OC-3
- STS-1□□OC-3 (Add/Drop)
- STS-1 (Bulk Filled) □□STS-1
- T3□□OC-3 (Internal and Add/Drop)
- T3□□STS-1 (Internal only)
- E1□□VT-2□□ STS-1 (Internal and Add/Drop)
- E1□□VT-2□□ OC-3 (Internal and Add/Drop)
- T1□□VT-1.5□□STS-1 (Internal and Add/Drop)

SDH

- VC-4 (Bulk filled)□□AU-4□□STM-1
- STM-0□□AU-3□□STM-1 (Add/Drop)
- VC-3 (Bulk Filled) □□AU-3□□STM-1
- T3□□AU-3□□STM-1 (Internal and Add/Drop)
- T3□□AU-3□□ STM-0 (Internal only)
- E1□□TU-12□□TUG-2□□AU-3□□STM-0
- E1□□TU-12□□TUG-2□□AU-3□□STM-1
- E1□□TU-12□□TUG-2□□TUG-3□□AU-4□□STM-1
- T1□□TU-11□□TUG-2□□AU-3□□STM-0
- T1□□TU-11□□TUG-2□□ AU-3□□STM-1

Other capabilities:

Monitor incoming TOH, POH. Monitor incoming APS messages (K1 and K2), Monitor incoming SPE pointers, Count Pointer Justifications, Detect NDF (New Data Flag) etc.

SDH

Alarm Detection: LOS, LOF, MS-AIS, MS-RDI, AU-LOP, AU-AIS, HP-RDI, HP-UNEQ, H4-LOM, TU-LOP, TU-AIS, LP-RDI, LP-UN-EQ

Error Counting: Framing error, B1 BIP, B2 BIP, MS-REI, B3 BIP, HP-REI, BERT errors

Signal Traces and Labels: Regenerator Section trace (J0), Higher Order trail trace (J1), Section sync status (S1), Path signal label (C2), LP Path label (V5)

Other capabilities: Monitor incoming RS-OH, MS-OH and HO-POH, Monitor incoming APS messages (K1 and K2), Monitor incoming AU pointers. Count Pointer Justifications, Detect NDF (New Data Flag) etc.

PDH

Alarm Detection: **T1:** AIS, OOF, RAI **E1:** AIS, OOF, RAI, CAS-MFL, RMFAI **T3:** LOS, FERF, OOF, AIS, IDLE, RED

Add/Drop Capabilities SONET

Add/Drop to/from OC-3: STS-1, T3, E1 or T1
Add/Drop to/from STS-1: T1 or E1

SDH

Add/Drop to/from STM-1: STM-0, T3, E1 or T1
Add/Drop to/from STM-0: T1 or E1

Frequency Measurements

SONET: OC-3 or STS-1 with 1Hz discrimination, 4.6ppm accuracy

SDH: STM-1 or STM-0 with 1Hz discrimination, 4.6ppm accuracy

PDH Framing Formats

DS3/T3: C-bit Parity, M23
DS1/T1: Unframed, D4, ESF
E1: Unframed, PCM30, PCM30CRC, PCM31, PCM31CRC

Alarm and Error Logging

Alarms and Errors can be logged continuously to a file.

Coupled or Independent Settings

Transmit and Receive settings can be set as coupled to change them simultaneously or they can be set as independent.

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Supported Protocols

TM – Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.

P over SONET (PoS) – Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).

C-3/OC-12/STM-1/STM-4 Transparent Payload – Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols.

System config example

Interfaces:

ual /Quad Ports

OC-3 / STM-1 / OC-12 / STM-4

x Gigabit Ethernet

ngle Mode or Multi Mode SFP support with LC connector

USB 2.0

cols:

C 2615 compliance

PoS compliance specs needed

Tx Clock

Internal or Recovered

LEDs:

LOS, LOF, User

Display Interface:

VGA/DVI

nbedded 8.4” LCD TFT Display

Power and Dimensions:

Factor: 19” Rackmount

0V/230V AC

19” (W) x 22”D x 7” H (4U)

Available Softwares

OC-3 / STM-1 Related Software

LTS200 – OC-3 / STM-1 ATM Monitor, BERT, Tx/Rx Test, RAW

LTS201 – OC-3 / STM-1 PoS Monitor, BERT, Tx/Rx Test, RAW

LTS202 – OC-3 / STM-1 ATM and RAW Record / Playback

LTS203 – OC-3 / STM-1 PoS and RAW Record / Playback

LTS204 – OC-3 / STM-1 ATM Protocol Analysis

LTS205 – OC-3 / STM-1 PoS Protocol Analysis

LTS206 – OC-3 / STM-1 UMTS Protocol Analysis

LTS207 – Delay Emulation for OC3 / STM1 PoS payloads

LTS208 – Delay Emulation for OC3 / STM1 ATM payloads

OC-12 / STM-4 Related Software

LTS300 – OC-12 / STM-4 ATM Monitor, BERT, Tx/Rx Test, RAW

LTS301 – OC-12 / STM-4 PoS Monitor, BERT, Tx/Rx Test, RAW

LTS302 – OC-12 / STM-4 ATM and RAW Record / Playback

LTS303 – OC-12 / STM-4 PoS and RAW Record / Playback

LTS304 – OC-12 / STM-4 ATM Protocol Analysis

LTS305 – OC-12 / STM-4 PoS Protocol Analysis

LTS306 – OC-12 / STM-4 UMTS Protocol Analysis

LTS307 – Delay Emulation for OC12 / STM4 PoS payloads

LTS308 – Delay Emulation for OC12 / STM4 ATM payloads

