OC3T3 19" rackmount TELCO NETWORK ANALYZER, OC-3/T3, STM-1, T1, E1 Analysis System

OC-3/T3,STM-1, STS-1/STM-0, T3, T1, E1 Interfaces

Add/Drop User-Selected PDH Signals to/from an OC-3/STM-1 or STS-1/STM-0

Add/Drop STS-1 to/from OC-3 or STM-0 to/from STM-1

Generate and Monitor SONET or SDH Alarms and Errors

Internally generate BERT patterns in all framing modes

DS0, DS1 or E1 Test and Analysis with GL's Ultra T1 or E1 Cards

DS3 Test and Analysis option

Multiple OC-3/STM-1 Channels in a system

Supports M23 and C-bit Framing Format

DS3/DS1/DS0 Test and

Analysis with UltraT1/E1

T3 line frequency and level

Measurement

Non-Intrusive Monitor for

Alarms and Errors

Drop and Insert User Selected

T1/E1

Broadcast or Looped back

individual DS1/E1

Decode and Simulate FEAC

And FDL Messages

Compatible with PCAP protocol

TNA OC-3/T3 System Overview

OC3T3 analyzer system is rugged a multichannel data/protocol analyzer emulator turnkey solution utilizing gl communications and other third party vendor components carefully assembled and packaged for analyzing, testing, simulating, and monitoring OC-3/T3/STM-1 and STS-1/STM-0 signals. The system can add and drop T1, E1, T3, or STS-1/STM-0 signals to and from an OC-3/STM-1 signal or T1 and E1 signals to and from an STS-1/STM-0 signal. The OC3T3 can also generate BERT patterns, internally in all framing modes. Accompanying Windows NT/2000/XP software affords easy operation. It is ideally suited for installation, maintenance, commissioning, verification and manufacturing of SONET/SDH transport networks and network equipment.

Benefits:

>Cost Effective: Most cost effective and expandable solution for SONET/SDH testing.

>Comprehensive: The OC-3/STM-1 and STS-1/STM-0 receivers monitor SONET/SDH signals and present in real-time comprehensive diagnostics of SONET/SDH alarms, errors and pointer justifications.

>PC Based: Open architecture, based on industry standard Windows O/S and easy to operate and do SONET/SDH analysis, testing, simulating, and monitoring platform. This will maximize the returns from your current investment on network testing.

>Complete Solution: 100% compatible with GL's Ultra T1 Card, Ultra E1 Card and Ultra T3 boards., the OC3T3 system provides a complete OC-3/STM-1, DS3, DS1, E1 and DS0 testing solution.

>Flexible: Use multiple channels or ports with a single central controlled by the same software, thereby providing the most flexible solution for your unique testing needs.

Features:

+Easy to use, familiar, windows based, Graphical User Interface

+Internally generate BERT patterns in all framing modes and perform stress test and performance analysis.

+Add/Drop T1, E1, T3, STS-1/STM-0 to/from OC-3/STM-1

+SONET/SDH overhead monitoring and control

SONET/SDH Alarm and Error generation/detection

Transmit user-selected T1 (or E1) while remaining T1s (or E1s) are looped back or broadcast, and transmit user-selected STS-1/STM-0 within OC-3/STM-1 while remaining STS-1s/STM-0s are broadcast or looped back

Internal, External, and Recovered clock sources

Remote control, scripting & automation using Client-Server technology

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OC3T3 SPECIFICATIONS*

Physical Interfaces

OC3T3	SC Connector
STS-1/STM-0/T3:	Male BNC Connector
T1/E1:	RJ48c Connector
External Clock:	MCX Connector
PC Interface:	PCI 2.1 Compliant

OC3T3 Line Interface

Physical Interface:	SC Connector
Fiber Pigtail:	Single mode, 1310 nm
Pulse Mask:	Meets ITU-T G.957 and Bellcore DR-253-CORE
Line Code:	NRZ
Output Clock Reference:	Recovered OC-3 Clock, External 19.44 MHz, or Internally Generated 155.52MHz ± 4.6ppm
Rx Sensitivity:	-31 dBm

STS-1/STM-0 Line Interface

Physical Interface:	BNC Male Connectors
Output Clock Reference:	Recovered STS-1/STM-0 Clock, External 19.44 MHz, or Internally Generated 51.84MHz ± 4.6ppm

T3 Line Interface

Physical Interface:	BNC Male Connectors
Line Code Format:	B3ZS
Framing Format:	M23, C-bit
Input Frequency:	44.736 Mbps
Receiver Interface:	DSX-3 (Terminate or Monitor)
Input Impedance:	75 Ohms
Input Level:	**Terminate**- 0.09 Vp – 0.85 Vp **Monitor** 0.025– 0.08 Vp (Up to 26 dB flat loss relative to nominal DSX)
Output Level:	**DSX**- Per TR-TSY-0004999, 0.75 to 0.85 Vp
Output Clock Source:	Recovered or Internal

T1/E1 Line Interface

Physical Interface:	RJ48c Connector
Line Code Format:	AMI or B8ZS (T1), HDB3 (E1)
Input Frequency:	1.544 Mbps (T1) or 2.048 Mbps (E1)
Receiver Interface:	Terminate
Input Impedance:	100 Ohms (T1), 120 Ohms (E1)
Input Level:	+75 mV to 6.0 V base to peak or –30 dBsX to +6 dBsX
Output Level:	+3.0 +/-0.2 Base to Peak Selectable 0 to 655 ft. Pulse Equalization Setting for T1 Short Haul, or line build outs for 0 dB to –22.5 dB (T1 Long Haul)

External Clock Interface

Physical Interface:	MCX Connector
Electrical Standard:	RS485/RS422

SONET/SDH Framing Formats

SONET: STS-3, STS-3c, STS-1
SDH: STM-1 (AU-3, AU-4)

Payload Mappings: SONET

- STS-3c (Bulk Filled) →OC-3
- STS-1→OC-3 (Add/Drop)
- STS-1 (Bulk Filled) →STS-1
- T3→OC-3 (Internal and Add/Drop)
- T3→STS-1 (Internal only)
- E1→VT-2→ STS-1 (Internal and Add/Drop)
- E1→VT-2→ OC-3 (Internal and Add/Drop)
- T1→VT-1.5→STS-1 (Internal and Add/Drop)
  T1→VT-1.5→ OC-3 (Internal and Add/Drop)

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SDH

- VC-4 (Bulk filled)→AU-4→STM-1
- STM-0→AU-3→STM-1 (Add/Drop)
- VC-3 (Bulk Filled) →AU-3→STM-1
- T3→AU-3→STM-1 (Internal and Add/Drop)
- T3→AU-3→ STM-0 (Internal only)
- E1→TU-12→TUG-2→AU-3→STM-0
- E1→TU-12→TUG-2→AU-3→STM-1
- E1→TU-12→TUG-2→TUG-3→AU-4→STM-1
- T1→TU-11→TUG-2→AU-3→STM-0
- T1→TU-11→TUG-2→ AU-3→STM-1
- T1→TU-11→TUG-2→TUG-3→AU-4→ STM-1
- T1→ TU-12→TUG-2→AU-3→STM-0
- T1→ TU-12→TUG-2→AU-3→ STM-1
- T1→ TU-12→TUG-2→TUG-3→AU-4→STM-1

  [All the E1 and T1 mappings support internal generation and Add/Drop]

Transmit Capabilities

Payload Source: Internally generated User Selected Pattern, Added from external source or Looped back from receive signal

Payload test patterns (Inverted or Non-inverted):

- **STS-1/STS-3c Bulk:** 2^{23}-1 PRBS
- **VC-3/VC-4 Bulk:** 2^{23}-1 PRBS
- **T3:** 2^{9}-1 PRBS, 2^{11}-1 PRBS, 2^{15}-1 PRBS, 2^{20}-1 PRBS, 2^{23}-1 PRBS
- **E1/T1:** QRSS, 2^{11}-1 PRBS, 2^{15}-1 PRBS, 2^{20}-1 PRBS

Alarm Generation SONET: LOS, LOF, AIS-L, RDI-L, LOP-P, AIS-P, RDI-P, UNEQ-P, LOM-P, LOP-V, AIS-V, RDI-V, UNEQ-V

SDH: LOS, LOF, MS-AIS, MS-RDI, AU-LOP, AU-AIS, HP-RDI, HP-UNEQ, H4-LOM, TU-LOP, TU-AIS, LP-RDI, LP-UNEQ

PDH: **T1:** AIS, RAI **E1:** LOF, AIS, RAI **T3:** LOS, AIS, IDLE

Error Insertion SONET: Framing error, CV-S, CV-L, REI-L, CV-P, REI-P, BERT errors (Single or Periodic error insertion capability)

SDH: Framing error, B1 BIP, B2 BIP, MS-REI, B3 BIP, HP-REI, BERT errors

Signal Traces and Labels:

SONET: Section trace (J0), Path trace (J1), Section sync status (S1), Path signal label (C2), VT Path signal label (C5)

SDH: Regenerator Section trace (J0), Higher Order trail trace (J1), Section sync status (S1), HP Path label (C2), LP Path label (V5)

Background Channel settings: Same as Foreground (Broadcast), Same as Received (Loopback), Unequipped or User Selected Pattern (Background VT payload)

Other capabilities: Set APS messages (K1 and K2), Monitor outgoing SPE/AU pointers

Receive Capabilities: SONET

Alarm Detection: LOS, LOF, AIS-L, RDI-L, LOP-P, AIS-P, RDI-P, UNEQ-P, LOP-V, LOM-P, AIS-V, RDI-V, UNEQ-V

Error Counting: Framing Error, CV-S, CV-L, REI-L, CV-P, REI-P, CV-V, REI-V, BERT errors

Signal Traces and Labels: Section trace (J0), Path trace (J1), Section sync status (S1), Path signal label (C2), VT Path signal label (C5)

Other capabilities:	Monitor incoming TOH, POH. Monitor incoming APS messages (K1 and K2), Monitor incoming SPE pointers, Count Pointer Justifications, Detect NDF (New Data Flag) etc.

SDH

Alarm Detection:	LOS, LOF, MS-AIS, MS-RDI, AU-LOP, AU-AIS, HP-RDI, HP-UNEQ, H4-LOM, TU-LOP, TU-AIS, LP-RDI, LP-UNEQ
Error Counting:	Framing error, B1 BIP, B2 BIP, MS-REI, B3 BIP, HP-REI, BERT errors
Signal Traces and Labels:	Regenerator Section trace (J0), Higher Order trail trace (J1), Section sync status (S1), Path signal label (C2), LP Path label (V5)
Other capabilities:	Monitor incoming RS-OH, MS-OH and HO-POH, Monitor incoming APS messages (K1 and K2), Monitor incoming AU pointers. Count Pointer Justifications, Detect NDF (New Data Flag) etc.

PDH

Alarm Detection:	**T1:** AIS, OOF, RAI **E1:** AIS, OOF, RAI, CAS-MFL, RMFAI **T3:** LOS, FERF, OOF, AIS, IDLE, RED

Add/Drop Capabilities : SONET

Add/Drop to/from OC-3:	STS-1, T3, E1 or T1
Add/Drop to/from STS-1:	T1 or E1

SDH

Add/Drop to/from STM-1:	STM-0, T3, E1 or T1
Add/Drop to/from STM-0:	T1 or E1

Frequency Measurements

SONET: OC-3 or STS-1 with 1Hz discrimination, 4.6ppm accuracy
SDH: STM-1 or STM-0 with 1Hz discrimination, 4.6ppm accuracy

PDH Framing Formats

DS3/T3:	C-bit Parity, M23
DS1/T1:	Unframed, D4, ESF
E1:	Unframed, PCM30, PCM30CRC, PCM31, PCM31CRC

Alarm and Error Logging

Alarms and Errors can be logged continuously to a file.

Coupled or Independent Settings

Transmit and Receive settings can be set as coupled to change them simultaneously or they can be set as independent.

Ordering Information

UT401 – Ultra OC-3 Card hardware (Option UT4010 and/or UT4020 required)
UT4010 – OC-3 Analysis Software
UT4020 – STM-1 Analysis Software

*Specifications and features subject to change without notice.

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